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10/826,886	04/15/2004	Richard David Taylor	MP2209-156672	1435

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EXAMINER	
RILEY, MARCUS T	

ART UNIT	PAPER NUMBER
2625	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/826,886	TAYLOR ET AL.	
	Examiner	Art Unit	
	MARCUS T. RILEY	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 February 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/15/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is responsive to applicant's remarks received on February 18, 2009. Claims 1-7 remain pending.

Response to Arguments

2. Applicant's arguments with respect to claims 1-7 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claim 1-3 & 6** are rejected under 35 U.S.C. 103(a) as being unpatentable over Amini '538 et al (US 5,381,538 hereinafter, Amini '538) in combination with Mills et al. (US 5,696,917 hereinafter, Mills '917).

Regarding claim 1; Amini '538 discloses a programmable interface comprising (*"Planar I/O interface circuit 112 controls the transferring and storing of information in PIO registers 114 as well as DMA control backup circuit 110.* ***Planar I/O interface circuit provides PIO programming information to and receives PIO programming information from PIO registers 114.***" column 10, lines 18-21):

a register file having a plurality of registers, each register having a type (See Figure 2 wherein #104 is a 20 byte FIFO and #114 is a PIO register);

a run control register (See Figure 3 wherein #114 is a PIO register *"PIO registers 114 store program information which is used during the operation of DMA controller 52. PIO registers include eight channels, corresponding to the eight channels of DMA controller 52. Each channel stores control information for a corresponding channel of DMA controller 52."* column 13, lines 32-40);

a Code Store SRAM, bidirectionally communicating with the microcontroller (See Figure 1 where #34 is the SRAM and #30 is the microprocessor within the processor portion #20. *"**Buffers 36, 38 are bidirectional, i.e., buffers 36, 38 can latch information which is provided by processor portion 20 and information which is provided to processor portion 20.** Because buffers 36, 38 are bidirectional, processor portion 20 may be replaced or upgraded while maintaining a standard base portion 22."* column 3, lines 19-25);

a microcontroller configured to bidirectionally communicate with the register file and the run control register (See Figure 1 where #34 is the SRAM and #30 is the microprocessor within the processor portion #20. *"**Buffers 36, 38 are bidirectional, i.e., buffers 36, 38 can latch information which is provided by processor portion 20 and information which is provided to processor portion 20.** Because buffers 36, 38 are bidirectional, processor portion 20 may be replaced or upgraded while maintaining a standard base portion 22."* column 3, lines 19-25);

wherein the Code Store SRAM and the run control register bidirectionally communicates with a system processor (See Figure 1 where #34 is the SRAM and #30 is the microprocessor within the processor portion #20. *"**Buffers 36, 38 are bidirectional, i.e., buffers 36, 38 can latch information which is provided by processor portion 20 and information which is provided to processor portion 20.** Because buffers 36, 38 are bidirectional, processor portion 20 may be replaced or upgraded while maintaining a standard base portion 22."* column 3, lines 19-25).

Amini '538 does not expressly disclose an executable code, loaded onto the Code Store RAM; wherein the system processor is configured to load the executable code onto the Code Store SRAM; and further configured to signal the microcontroller, via the run control register, to begin execution of one or more instructions included in the executable code.

Mills '917 discloses and executable code, loaded onto the Code Store RAM (*"In such a case, **the program associated with the selected game will be loaded into SRAM 240**... Moreover, the read/write files **(including the executable code for the game) stored in battery backed SRAM 240 will not be lost.**"* column 10, lines 33-53);

wherein the system processor is configured to load the executable code onto the Code Store SRAM and further configured to signal the microcontroller, via the run control register, to begin execution of one or more instructions included in the executable code (*"In such a case, **the program associated with the selected game will be loaded into SRAM 240**... Moreover, the read/write files **(including the executable code for the game) stored in battery backed SRAM 240 will not be lost.**"* column 10, lines 33-53); See also (*"... a **cache line of internal cache 215 of microprocessor 210 can be filled from SRAM 240** faster than would be the **case if a DRAM based main memory was used.** Also, programs **executing from SRAM 240 can be accessed, and hence executed,** faster than would be the case if a DRAM based memory was used.."* column 12, lines 11-16).

Amini '538 and Mills '917 are combinable because they are from same field of endeavor of communication systems (*"The present invention pertains to the field of the architecture of computer systems..."* Mills '917 at column 1, lines 7-8).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the communication system as taught by Amini '538 by adding an executable code, loaded onto the Code Store RAM; wherein the system processor is configured to load the executable code onto the Code Store SRAM; and further configured to signal the microcontroller, via the run control register, to begin execution of one or more instructions included in the executable code as taught by Mills '917. The motivation for doing so would have been because it advantageous to enable flash memory to operate in an optimal synchronous fashion with any synchronous bus to provide a low cost and to eliminate the time required to transfer code and data from the hard disk to the main memory. (*"It is also an object of this invention to enable flash memory to operate in an optimal synchronous fashion with any synchronous bus to provide a low cost, low power*

alternative to volatile main memory, and to eliminate the time required to transfer code and data from the hard disk to the main memory." Mills '917 at column 6, lines 56-61). Therefore, it would have been obvious to combine Amini '538 with Mills '917 to obtain the invention as specified in claim 1.

Regarding claim 4; Amini '538 discloses a device wherein the register type further includes FIFO registers, operative to communicate with a direct memory access controller (See Figure 2 where Fig. 2 is a schematic block diagram of a DMA controller and Figure 3 is a schematic block diagram of a portion of the Fig. 2 DMA controller. See Figure 4 where Fig. 4 is a schematic block diagram of the FIFO circuits of the DMA controller of Figs. 2 and 3.)

Regarding claim 7; Amini '538 discloses a device wherein the system processor is configured to bidirectionally communicate with the register file (See Figure 1 where #34 is the SRAM and #30 is the microprocessor within the processor portion #20. *"**Buffers 36, 38 are bidirectional, i.e., buffers 36, 38 can latch information which is provided by processor portion 20 and information which is provided to processor portion 20.** Because buffers 36, 38 are bidirectional, processor portion 20 may be replaced or upgraded while maintaining a standard base portion 22."* column 3, lines 19-25);

5. **Claims 2, 3 & 6** are rejected under 35 U.S.C. 103(a) as being unpatentable over Amini '538 and Mills '917 as applied to claim 1 above, and further in view of Curry et al. (US 6,112,275 hereinafter, Curry '275).

Regarding claim 2; Amini '538 as modified does not expressly disclose a device wherein the types of the registers are selected from a group that includes timer, General purpose, external I/O, internal I/O, shared, and interrupt.

Curry '275 discloses a device wherein the types of the registers are selected from a group that includes timer, General purpose, external I/O, internal I/O, shared, and interrupt (See Figure 21

wherein Fig. 21 shows register 2104 and Figures 22A-N show the schematic circuit, timing, and state diagrams of the embodiment of Fig. 21. *"Further preferred embodiment circuitry for chips 0130 and 0130' in the modules of FIGS. 1A-B are shown schematically in FIGS. 21, 22A, 22B, 22D, and 22G. FIG. 21 is a top level schematic of the embodiment, denoted generally 2100, which includes a* ***single input-output terminal IO****, a 1-wire converter 2102, an 8-bit command shift register 2104, a command decoder 2106, ROM and control 2108, secure RAM 2110, multiplexer 2112, power supply battery 2114, and battery test circuit 2116. Embodiment 2100 receives and* ***transmits serially over the IO terminal****..."* column 36, lines 52-56).

Amini '538 and Curry '275 are combinable because they are from same field of endeavor of communication systems (*Method of communicating..."* Curry '275, See Title).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the communication system as taught by Amini '538 by adding discloses a device wherein the types of the registers are selected from a group that includes timer, General purpose, external I/O, internal I/O, shared, and interrupt as taught by Curry '275. The motivation for doing so would have been because it advantageous to provide higher functionality at lower cost in a more compact package. (*"One of the long-term trends in electronics has been to provide higher functionality at lower cost in a more compact package."* Curry '275 at column 2, lines 17-19). Therefore, it would have been obvious to combine Amini '538 with Curry '275 to obtain the invention as specified in claim 1.

Regarding claim 3; Curry '275 discloses a device wherein when one of the registers has a type of external I/O, the register including edge detect logic (See Figures 9A-9B which shows the control logic used, in the presently preferred embodiment. *"****FIGS. 9A and 9B are two parts of a single Figure which shows the control logic used,*** *in the presently preferred embodiment, in the integrated circuit of FIG. 6. After the protocol register 920 has been loaded, counter chain 910 counts successive clock pulses. (****Every falling edge on the data line will lead to a clock pulse within the module, and these pulses are counted by counter 920.)*** *The counter 910 is also connected to logic which will intercept the clock signal (to freeze the count), and activate signal 210, as soon as 256 bits of data have been read or written. (Note that the counter chain shown actually includes two more stages than are needed. This permits ready modification for 1024-bit*

embodiments.) ***Register 920 receives the protocol word. The stages of this register are connected so that a RESET will set the first stage, and clear the other stages. Thus, when a 1 propagates through to the last stage, a protocol word has been loaded.*** *"* column 15, lines 64-67 thru column 16, lines 1-13).

Regarding claim 6; Curry '275 discloses a device wherein the executable code is selected from a group that includes serial interfaces, parallel interfaces, serial peripheral interface (SPI), Synchronous Serial Interface (SSI), MicroWire, Inter Integrated Circuit (I2C), control area network (CAN), UART, IEEE1284, LCD interface, front panel interface, and MODEM (*"To interface to this protocol,* ***the programmable capabilities of the standard UART chip in the computer's RS232 interface are exploited to provide adaptation to the time base requirements of the module.*** *This is done by writing an entire byte of output from the UART, at a much higher baud rate than the module can be relied on to accept, to write a single bit of data into the module.* ***The read-data line (RX) of the UART is tied back to the transmit-data line (TX) through a resistor****, so that the UART will also always report a read of the same data byte being written, unless the token has turned on its pull-down transistor."* column 10, lines 18-28).

6. **Claim 5** is rejected under 35 U.S.C. 103(a) as being unpatentable over Amini '538 and Mills '917 as applied to claim1 above, and further in view of Ueda (US 5,631,637 hereinafter, Ueda '637).

Regarding claim 5; Amini '538 as modified does not expressly disclose a device wherein the executable code implements a laser printer mechanism communications interface and a vertical top-of-page synchronization interface.

Ueda '637 discloses a device wherein the executable code implements a laser printer mechanism communications interface and a vertical top-of-page synchronization interface (*"When* ***the printing data of a page are developed in the bit map memory 17, the main control unit 18 sends a printing start signal 121 to a printing mechanism shown in FIG. 2.*** *Said printing mechanism is of so-called raster scanning type,* ***such as a laser beam***

***printer**, and releases a horizontal synchronization (BD) signal 122 and a vertical synchronization signal 123 when the printing operation is enabled."* column 4, lines 7-14).

Amini '538 and Ueda '637 are combinable with because they are from same field of endeavor of communication systems (*"The present embodiment has been explained by a configuration employing a laser beam printer, but the present invention is not limited to such configuration and is applicable to any equipment that can effect wireless or cable exchange of data with an external equipment, such as a printer of other types, a display apparatus, a memory apparatus or a communication apparatus."* Smith '733 at column 6, lines 6-12).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the communication system as taught by Amini '538 and Ueda '637 by adding a device wherein the executable code implements a laser printer mechanism communications interface and a vertical top-of-page synchronization interface as taught by Ueda '637. The motivation for doing so would have been because it advantageous to provide an output apparatus for receiving data from an external equipment (*"Still another object of the present invention is to provide an output apparatus for receiving data from an external equipment..."* Smith '733 at column 2, lines 3-6). Therefore, it would have been obvious to combine Amini '538 with Ueda '637 to obtain the invention as specified in claim 1.

Examiner Notes

7. The Examiner cites particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested that, in preparing responses, the applicant fully considers the references in its entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or as disclosed by the Examiner.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MARCUS T. RILEY whose telephone number is (571)270-1581. The examiner can normally be reached on Monday - Friday, 7:30-5:00, est.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David K. Moore can be reached on 571-272-7437. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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